

Advanced Chip Design Practical Examples In Verilog

SystemVerilog for Design Second Edition A Practical Guide for SystemVerilog Assertions Learning from VLSI Design Experience Verilog Quickstart Java by Example Rapid Prototyping of Digital Systems Formal Methods in Computer-aided Design IEEE Circuits & Devices Specification-driven Functional Verification with Verilog PLI & VPI and SystemVerilog DPI Java Studio by Example Verilog Computer-Based Training Course Effective VisualAge for Java, Version 3 Core Java ACM SIGPLAN Notices Proceedings of the ... IEEE International Caracas Conference on Devices, Circuits and Systems Proceedings Reuse Methodology Manual for System-on-a-chip Designs Instant Java Linux Journal Advances in Hardware Design and Verification Stuart Sutherland Srikanth Vijayaraghavan Weng Fook Lee James M. Lee Jerry R. Jackson James O. Hamblen Suraj N. Kurapati Lynn Weaver Zainalabedin Navabi Scott Stanchfield Gary Cornell Michael Keating John A. Pew Hon Li

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systemverilog is a rich set of extensions to the ieee 1364 2001 verilog hardware description language verilog hdl these extensions address two major aspects of hdl based design first modeling very large designs with concise accurate and intuitive code second writing high level test programs to efficiently and effectively verify these large designs the first edition of this book addressed the first aspect of the systemverilog extensions to verilog important modeling features were presented such as two state data types enumerated types user defined types structures unions and interfaces emphasis was placed on the proper usage of these enhancements for simulation and synthesis systemverilog for design second edition has been extensively revised on a chapter by chapter basis to include the many text and example updates needed to reflect changes that were made between the first edition of this book was written and the finalization of the new standard it is important that the book reflect these syntax and semantic changes to the systemverilog language in addition the second edition features a new chapter that explains the systemverilog packages a new appendix that summarizes the synthesis guidelines presented throughout the book and all of the code examples have been updated to the final syntax and rerun using the latest version of the synopsys mentor and cadence tools

systemverilog language consists of three very specific areas of constructs design assertions and testbench assertions add a whole new dimension to the asic verification process assertions provide a better way to do verification proactively traditionally engineers are used to writing verilog test benches that help simulate their design verilog is a procedural language and is very limited in capabilities to handle the complex asic s built today systemverilog assertions sva are a declarative and temporal language that provides excellent control over time and parallelism this provides the designers a very strong tool to solve their verification problems while the language is built solid the thinking is very different from the user s perspective when compared to standard verilog language the concept is still very new and there is not enough expertise in the field to adopt this methodology and be successful while the language has been defined very well there is no practical guide that shows how to use the language to solve real verification problems this book will be the practical guide that will help people to understand this new methodology today s soc complexity coupled with time to market and first silicon success pressures make assertion based verification a requirement and this book points the way to effective use of assertions satish s iyengar director asic engineering crimson microsystems inc this book benefits both the beginner and the more advanced users of systemverilog assertions sva first by introducing the concept of assertion based verification abv in a simple to understand way then by discussing the myriad of ideas in a broader scope that sva can accommodate the many real life examples provided throughout the book are especially useful irwan sie director ic design ess technology inc systemverilogassertions is a new language that can find and isolate bugs early in the design cycle this book shows how to verify complex protocols and memories using sva with several examples this book is a good reference guide for both design and verification engineers derick lin senior director engineering airgo networks inc

this book shares with readers practical design knowledge gained from the author s 24 years of ic design experience the author addresses issues and challenges faced commonly by ic designers along with solutions and workarounds guidelines are described for

tackling issues such as clock domain crossing using lockup latch to cross clock domains during scan shift implementation of scan chains across power domain optimization methods to improve timing how standard cell libraries can aid in synthesis optimization bkm best known method for rtl coding test compression memory bist usage of signed verilog for design requiring ve and ve calculations state machine code coverage and much more numerous figures and examples are provided to aid the reader in understanding the issues and their workarounds

from a review of the second edition if you are new to the field and want to know what all this verilog stuff is about you ve found the golden goose the text here is straight forward complete and example rich mega multi kudos to the author james lee though not as detailed as the verilog reference guides from cadence it likewise doesn t suffer from the excessive abstractness those make you wade through this is a quick and easy read and will serve as a desktop reference for as long as verilog lives best testimonial i m buying my fourth and fifth copies tonight i ve loaned out lost two of my others zach coombes amd

this book highlights key features of the java language with examples designed for experienced programmers the text clearly and concisely describes how to create java applets and applications and shows the development of a complete java program from start to finish the cd rom includes all java source code examples from the book java applets the latest release of the java developer s kit and cafe lite

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software programming languages

the asian test symposium provides an international forum for engineers and researchers from all countries of the world especially from asia to present and discuss various aspects of system board and device testing with design manufacturing and field considerations in mind ats 2003 s papers shares state of the art ideas and technologies in testing

silicon technology now allows us to build chips consisting of tens of millions of transistors this technology not only promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer as a result many asic developers and silicon vendors are re examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available design reuse the use of pre designed and pre verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity reuse methodology manual for system on a chip designs second edition outlines an effective methodology for creating reusable designs for use in a system on a chip soc design methodology silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem instead this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process

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